Curriculum Vitae

HARDUS RICHTER

29 Viljoen Way

Pierre van Ryneveld

Centurion

0157

PERSONAL INFORMATION

Date of Birth	1990-12-07
Nationality	South African
Telephone Number	079 495 9064
Email Address	hardus_richter@hotmail.com
Driving Licence	Code 8
Marital Status	Married
Criminal Record	None

EDUCATION

HIGH SCHOOL CENTURION
Grade 12 Achieved 2009

Subjects	Afrikaans, English, Mathematics, Physical Science, Information Technology, Electrical Technology, Life Orientation
	Obtained distinctions in all subjects
Additional subject	Mathematics 3: probability, data handling & geometry

UNIVERSITY OF PRETORIA

Bachelor of Engineering, Computer Engineering

Dean's Merit List 2010
Golden Key Award 2011
Merit Award (Bronze) for Third Year Study in Computer Engineering 2012
Dean's Merit List 2012
Obtained with distinction 2013, 78% average

Bachelor of Engineering Honours, Computer Engineering

Obtained with distinction 2014, 83% average

Master of Engineering, Computer Engineering

Obtained with distinction 2019, 88% average

EXPERIENCE

TELKOM

Job Title	Vacation Training
Employer	Technical Product Development, Telkom
Period	January 2013
Description of Duties	I was involved with the development and implementation of a machine learning based prototype system for the stabilization of the DSL network.

UNIVERSITY OF PRETORIA

Job Title	Assistant Lecturer
Employer	Faculty of Engineering, Built Environment & IT, University of Pretoria
Period	January 2014 to December 2015
Description of Duties	I was involved with the first year electricity and electronics subject (EBN 111). My responsibilities included: • The supervision and assistance of students during practical sessions. • Compilation of practical work. • Assistance of students during tutorial sessions. • Grading of tests. I was also involved with design and development of a robotics platform to educate High School students (Robotics Academy). My primary focus in this area is the design and implementation of the localisation system, diagnostic tools and teleoperation system.

ASIC DESIGN SERVICES

Job Title	Machine Learning Engineer
Employer	ASIC Design Services
Period	January 2016 to present
Description of Duties	I am the lead machine learning engineer and software developer for the Core Deep Learning (https://coredeeplearning.ai/) project. Core Deep Learning is a Deep Learning platform for FPGAs where the IP Core is optimized for the application's deep neural network and the target FPGA. In this respect my responsibilities includes: • Development of complete machine learning and computer vision applications to meet end user requirements. • Integration of our own software flow with common machine learning frameworks such as TensorFlow and Caffe. • Research and development of methods to quantize neural networks to 8-bit with minimal accuracy loss. • Development of an optimization framework to search through millions to billions of FPGA IP Core configurations to find optimal solutions. • Development of PC communication drivers to communicate with the FPGA through Ethernet, Serial and PCI Express protocols. Furthermore I regularly engage with international customers through video calls, on the showfloor at trade shows and direct meetings. I have also been involved in the development of communication protocols on ARM Cortex-M3 and RISC-V embedded processors.

KEY SKILLS

Development of Computer Vision and Deep Learning solutions.
Proficient in the Caffe, TensorFlow and Keras Deep Learning Frameworks.
Research, evaluation and development of solutions to novel problems.
Proficient in Python, C, and C++.
Algorithm development and optimization for performance and efficiency.
Multi-threaded CPU and CUDA based GPU software development.

REFERENCES

Name	Mr Robert Green
Relation	Former colleague at ASIC Design Services
Position	Embedded Design and Software Engineer Reutech Solutions
Phone Number	084 817 8058
Email Address	robertg@reutech.co.za